Maharashtra State Board of Technical Education, Mumbai
TEACHING PLAN (TP)

K-1

Academic Year: 2026-27 **Date:** 29/06/2026
Institute Name & Code: K. K. Wagh Polytechnic, Nashik-3 (0078)
Program and Code: Artificial Intelligence & Machine Learning (AN) **Course Code &. Abbr.:** 313303 (DTE)
Course Name: Digital Techniques (DTE) **Name of Faculty:** Ms. K. J. Patil
Class: SYAN- NEURAL **Total Hrs:** 30 **Course Index:** CO302 **Semester:** III **Scheme:** K

● Teaching and Examination Scheme:

Course Code	Course Title	Abbr	Course Category/s	Learning Scheme					Credits	Paper Duration	Assessment Scheme										Total Marks
				Actual Contact Hrs/Week			SLH	NLH			Theory				Based on LL & TSL Practical				Based on SL		
											FA-TH	SA-TH	Total		FA-PR		SA-PR		SLA		
				CL	TL	LL					Max	Max	Max	Min	Max	Min	Max	Min	Max	Min	
313303	Digital Techniques	DTE	DSC	3	-	2	1	6	3	3	30	70 *#	100	40	25	10	25#	10	25	10	175

Abbreviations: CL- Class Room Learning , TL- Tutorial Learning, LL-Laboratory Learning, SLH-Self Learning Hours, NLH-Notional Learning Hours, FA - Formative Assessment, SA -Summative assessment, IKS - Indian Knowledge System, SLA - Self Learning Assessment
Legends: @ Internal Assessment, # External Assessment, *# On Line Examination , @$ Internal Online Examination

● Course Outcomes (COs): Theory & Practical

By learning course Digital Techniques (DTE-313303) Second Year students will be able to:

- CO1 - Apply number system and codes concept to interpret working of digital systems.
- CO2 - Apply Boolean laws to minimize complex Boolean function.
- CO3 - Develop combinational logic circuits for given applications.
- CO4 - Develop sequential logic circuits using Flip-flops.
- CO5 - Interpret the functions of data converters and memories in digital electronic systems.

CO No.	TLO No.	Course Outcomes (COs) / Theory Learning Outcomes (TLOs)
CO302.1(CO1)		**CO1 - Number Systems**
	TLO 1.1	Convert the given number from one number system to another number system.
	TLO 1.2	Perform arithmetic operations on binary numbers.
	TLO 1.3	Subtract given binary numbers using 1's and 2's compliment method.
	TLO 1.4	Convert the given coded number into the other specified code.
	TLO 1.5	BCD Arithmetic: BCD Addition, Subtraction using 9's and 10's complement
CO302.2(CO2)		**CO2 - Logic Gates and Boolean Algebra**
	TLO 2.1	Define the given characteristics parameters of the digital logic families.
	TLO 2.2	Draw symbol and truth table of given logic gates.
	TLO 2.3	Explain the concept of Buffer and Tristate logic .
	TLO 2.4	Implement basic gates and other gates with the help of universal gates.
	TLO 2.5	Simplify the given expression using Boolean laws and develop logic circuits .
CO302.3(CO3)		**CO3 - Combinational Logic Circuits**
	TLO 3.1	Develop logic circuits for standard SOP/POS form of the given logic expression.
	TLO 3.2	Minimize the given logic expression using K-map (up to 4 variables).
	TLO 3.3	Design Adder and subtractor using K-map.

	TLO 3.4	Describe working of specified Encoder and Decoder with help of block diagram and truth table.
	TLO 3.5	Describe the working of Multiplexer and Demultiplexer.
CO302.4(CO4)		**CO4 - Sequential Logic Circuits**
	TLO 4.1	Differentiate between Latch and Flip Flop.
	TLO 4.2	Explain basic memory cells and use relevant triggering techniques for the given digital circuit.
	TLO 4.3	Describe the truth tables for the given Flip flops, applications of Flip flops.
	TLO 4.4	Use the given type of flip flop and its excitation table to design a specific type of counter.
	TLO 4.5	Describe the working of specified shift register with the help of a timing diagram.
	TLO 4.6	Design specified modulo-N counter using Flip flops
	TLO 4.7	Design Ring /Twisted ring counter using a given Flip-Flop.
CO302.5(CO5)		**CO5 - Data Converters and Memories**
	TLO 5.1	Describe the working of the given type of DAC.
	TLO 5.2	Calculate the output voltage for the given digital input for specified DAC.
	TLO 5.3	Describe the working of the given type of ADC.
	TLO 5.4	Compare the working of ROM,EPROM, EEPROM and Flash Memory .

- **Teaching Plan:**
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Chapter No. (Alloted Hrs.)	TLOs	Title/Topic Details with CO	Plan (From-To & No. of Lectures)	Actual Execution (From-To & No. of Lectures)	Teaching Method/ Media	Remark
01 (05)		**Unit 1: Number Systems**				
	1.1	1.1 Number Systems: Types of Number Systems (Binary, Octal, Decimal, Hexadecimal), conversion of number systems	03/07/2026 (01)		Chalk,Board + LCD Projector + PPT Presentations + MKCL ERA LMS	
	1.2	1.2 Binary Arithmetic: Addition, Subtraction, Multiplication and Division	04/06/2026 (01)			
	1.3	1.3 Subtraction using 1's and 2's complement method	07/07/2026 (01)			
	1.4	1.4 Codes: BCD, Gray code, Excess-3 and ASCII code,Code conversions, Applications of codes.	10/07/2026 (01)			
	1.5	1.5 BCD Arithmetic: BCD Addition, Subtraction using 9's and 10's complement	11/07/2026 (01)			
02 (08)		**Unit 2: Logic Gates and Boolean Algebra**				
	2.1	2.1 Logic Families: Characteristics Parameters of logic Families- Noise margin, Power dissipation, Figure of merit ,Fan in, Fan out, Speed of operation, maximum clock frequency supply voltage requirement ,power per gate , Comparison of TTL, CMOS and ECL logic family	14/07/2026 TO 17/07/2026 (02)			
	2.2	2.2 Introduction to positive and negative logic systems, Logic Gates: Symbol ,Truth table of Basic logic gates(AND,OR,NOT),Universal gates(NAND,NOR) and Special purpose gates(EX-OR,EX-NOR)	18/07/2026 TO 21/07/2026 (02)			
	2.3	2.3 Buffer: Tristate logic, Unidirectional and Bidirectional	24/07/2026 TO 25/07/2026 (02)			

	2.4	2.4 Boolean algebra : Laws of Boolean algebra, Duality Theorem ,De-Morgan's theorem	28/07/2026 TO 31/07/2026 (02)			
03 (12)		**Unit 3: Combinational Logic Circuits**				
	3.1	3.1 Standard Boolean expression: Sum of products [SOP] and Products of Sum [POS], Min-term and Max-term	01/08/2026 TO 04/08/2026 (02)		Chalk,Board + LCD Projector + PPT Presentations + MKCL ERA LMS	
	3.1	3.2 SOP-POS form conversion, realisation using NAND/NOR gates	07/08/2026 (1)			
	3.2	3.2 Boolean Expression reduction using K-map: Minimization of Boolean expressions (upto 4 variables) using SOP and POS form	08/08/2026 TO 11/08/2026 (02)			
	3.3	3.3Arithemetic circuits : design Half and Full Adder using K-maps, design Half and Full Subtractor using K-maps , n bit adder and n bit subtractor .	14/08/2026 TO 18/08/2026 (02)			
	3.4	3.4 Encoder and Decoder: Functions of Encoder and Decoder, Block Diagram and Truth table, Priority Encoder (4:2, 8:3)	21/08/2026 TO 22/08/2026 (02)			
	3.4	3.4 BCD to 7 segment Decoder/Driver, Keyboard Encoder / decoder	25/08/2026 (1)			
	3.5	3.5 Multiplexer and Demultiplexer: Working, Truth table and applications of MUX and DEMUX. MUX tree, DEMUX tree, DEMUX as Decoder	28/08/2026 TO 29/08/2026 (02)			
04 (12)		**Unit 4: Sequential Logic Circuits**				
	4.1	4.1 Difference between Combinational and Sequential Logic circuits, Time independent (un-clocked)and Time dependent (Clocked) logic system , Flips- Flops and Latch, Basic memory cell ,RS-Latch using NAND and NOR,	01/09/2026 To 04/09/2026 (02)			
	4.1	4.1 Triggering methods- Edge trigger and Level Trigger	05/09/2026 (01)			
	4.2	4.2 Flip-Flops: S-R, J-K, T and D, Truth table and logic circuits of each flip-flop, Excitation table, applications	08/09/2026 To 11/09/2026 (02)			
	4.3	4.3 Race around condition in JK flip-flop, Master-Slave JK Flip Flop	12/09/2026 To 15/09/2026 (02)			
	4.4	4.4 Shift registers- Serial In Serial Out, Serial In Parallel Out, Parallel In Serial Out ,Parallel In Parallel Out,Bi-directional Shift register, 4-bit Universal Shift register	18/09/2026 To 19/09/2026 (02)			
	4.5	4.5 Counters- Synchronous and Asynchronous counters, Modulus of counter, Ripple counter, Ring Counter, Twisted Ring Counter, Up – down counter,	22/09/2026 To 25/09/2026 (02)			
	4.5	Decade Counter, MOD-N counter, Timing Diagram	26/09/2026 (01)			
		Unit 5: Data Converters and Memories				
	5.1	5.1 Digital to Analog Data Converter (DAC)-circuit diagram and working of Weighted resistor	29/09/2026 To 03/10/2026			

05 (08)		DAC and R-2R Ladder DAC, DAC Specification/Selection factors	(02)		Chalk,Board + LCD Projector + PPT Presentations + MKCL ERA LMS	
	5.2	5.2 Analog to Digital Data Converter (ADC) : Block Diagram, Types and Working of Dual Slope ADC, Successive Approximation, Flash Type ADC, ADC selection factors/ specifications	06/10/2026 To 09/10/2026 (02)			
	5.3	5.3 Memories: Types- Primary memory , Secondary Memory, Organization, Dimension, Memory Bank, Features , Applications: RAM (SRAM, DRAM), Volatile and Non-Volatile, ROM (PROM, EPROM, EEPROM), Flash Memory, Comparison of RAM and ROM,EPROM and Flash Memory, SIMM: Features, SSD memory: Features,	10/10/2026 To 13/10/2026 (02)			
	5.3	5.4 Comparison of RAM and ROM,EPROM and Flash Memory, SIMM: Features, SSD memory: Features,	16/10/2026 (01)			
		Total	**45 Hrs.**			

● Chapter wise CO-PO Mapping:

Course Outcomes (COs)	Programme Outcomes (POs)							Programme Specific Outcomes PSOs	
	PO-1 Basic and Discipline Specific Knowledge	PO-2 Problem Analysis	PO-3 Design/ Development of Solutions	PO-4 Engineering Tools	PO-5 Engineering Practices for Society, Sustainability and Environment	PO-6 Project Management	PO-7 Life Long Learning	PSO-1	PSO-2
CO1	2	-	1	-	-	-	3	1	2
CO2	2	-	2	-	-	-	2	2	2
CO3	3	2	3	2	-	1	2	1	1
CO4	3	2	3	2	-	1	2	1	1
CO5	2	-	2	2	1	1	2	2	1

Legends :- High:03, Medium:02,Low:01, No Mapping: -

● Formative assessment (Assessment for Learning) :

- Two offline unit tests of 30 marks and average of two unit test marks will be considered for out of 30 marks.
- Each practical will be assessed considering 60% weightage to process, 40% weightage to product.
- For formative assessment of laboratory learning 25 marks

● Summative Assessment (Assessment of Learning)

- End semester assessment of 70 marks.
- End semester summative assessment of 50 marks for laboratory learning

- **References:**

1. **Books:**

Sr no	Author	Title	Publisher
1	Jain R.P	Modern Digital Electronics	McGraw-Hill Publishing, New Delhi,2009 ISBN:9780070669116
2	Anand Kumar	Fundamentals of Digital Circuits	PHI learning Private limited, ISBN:978-81-203-5268-1
3	Salivahanan S, Arivazhagan S.	Digital Circuits and Design	Vikas Publishing House, New Delhi,2013 ISBN: 9789325960411
4	Puri.V.K	Digital Electronics	McGraw-Hill Publishing, New Delhi,2016 ISBN:97800746331751
5	Malvino A.P Donald .P. Leach	Digital Principles	McGraw-Hill Education, New Delhi ISBN:9789339203405
6	Anil.K.Maini	Digital Electronics: Principles, Devices and Applications	Wiley India, Delhi, 2007, ISBN:9780470032145

2. Web Sites:

Sr. No	Link /Portal	Description
1	https://studytronics.weebly.com/digital-electronics.html	Basics of Digital Electronics
2	https://www.udemy.com/course/basics-of-digital-techniques/	Introduction To Digital Number System & Logic Gates
3	https://www.geeksforgeeks.org/synchronous-sequential-circuits-in-digital-logic/	Boolean Algebra and Logic Gates, Combinational and Sequential Logic Circuits
4	https://onlinecourses.nptel.ac.in/noc19_ee51/preview	Digital Circuits
5	https://de-iitr.vlabs.ac.in/	Virtual Labs for Digital Systems
6	https://www.tutorialspoint.com/digital_circuits/digital_circuits_sequential_circuits.htm	Sequential Circuits

Ms. K.J. Patil
(Name & signature of staff)

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