Maharashtra State Board of Technical Education, Mumbai
LABORATORY PLANNING (LP)

K2-A

Academic Year: 2026-27 **Date:** 30/06/2026
Institute Name & Code: K. K. Wagh Polytechnic, Nashik-3 (0078)
Program and Code: Artificial Intelligence & Machine Learning (AN) **Course Code &. Abbr.:** 313303 (DTE)
Course Name: Digital Techniques (DTE) **Name of Faculty:** Ms. K. J. Patil
Class: SYAN- NOVA **Total Hrs:** 30 **Course Index:** CO302 **Semester:** III **Scheme:** K

● Course Outcomes (COs): Theory & Practical

By learning course Digital Techniques (DTE-313303) Second Year students will be able to:

- CO1 - Apply number system and codes concept to interpret working of digital systems.
- CO2 - Apply Boolean laws to minimize complex Boolean function.
- CO3 - Develop combinational logic circuits for given applications.
- CO4 - Develop sequential logic circuits using Flip-flops.
- CO5 - Interpret the functions of data converters and memories in digital electronic systems.

● Teaching and Examination Scheme:

Course Code	Course Title	Abbr	Course Category/s	Learning Scheme					Credits	Paper Duration	Assessment Scheme										
				Actual Contact Hrs/Week							Theory				Based on LL & TSL Practical				Based on SL		Total Marks
											FA-TH		SA-TH		Total		FA-PR		SA-PR		SLA		
				CL	TL	LL	SLH	NLH			Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	
313303	Digital Techniques	DTE	DSC	3	-	2	1	6	3	3	30	70*#	100	40	25	10	25#	10	25	10	175

Abbreviations: CL- Class Room Learning , TL- Tutorial Learning, LL-Laboratory Learning, SLH-Self Learning Hours, NLH-Notional Learning Hours, FA - Formative Assessment, SA -Summative assessment, IKS - Indian Knowledge System, SLA - Self Learning Assessment
Legends: @ Internal Assessment, # External Assessment, *# On Line Examination , @$ Internal Online Examination

● Laboratory Learning Outcome (LLO)

LLO	Practical -Laboratory Learning Outcome (LLO)
LLO 1.1	Test the functionality of basic gates.
LLO 2.1	Test the functionality of NAND and NOR gate using a breadboard.
LLO 3.1	Test the functionality of the constructed Basic gates using universal gates.
LLO 4.1	Construct Ex-OR, EX- NOR gates using universal gates.
LLO 5.1	Build the logic circuit on a breadboard to verify the De -Morgan's theorems.
LLO 6.1	Verify the truth table of Half and Full adder circuits for the given input
LLO 7.1	Verify the truth table of Half and Full subtractor using Boolean expressions.
LLO 10.1	Build / test function of MUX Digital IC.

. LLO 11.1	Build / test function of DEMUX Digital IC.
LLO 12.1	Test functionality of RS flip flop using NAND Gate .
LLO 13.1	Test functionality of Master Slave (MS) JK flip-flop using Digital IC.
LLO 14.1	Test functionality and truth table for D and T Flip flop.
LLO 16.1	Interpret timing diagram of 4-bit ripple counter using Digital IC.
LLO 17.1	Interpret timing diagram of Decade counter (Mod-10).
LLO 18.1	Build R-2R resistive network on breadboard to convert given digital data into analog.

- **Practical Plan**:

Sr. No	COS	Practical -Laboratory Learning Outcome (LLO)	Practical Titles	Date of Plan		Remark	Faculty Sign with Assessment Date
				From	To		
1	CO1 CO2	LLO 1.1 LLO 1.2	* Test the functionality of AND, OR, NOT, Ex-OR and EX-NOR logic Gates using equivalent 74 series or CMOS Devices [CD] series.	A:07/07/2026 B:01/07/2026 C:06/07/2026	A:14/07/2026 B:08/07/2026 C:13/07/2026		
2	CO2	LLO 2.1	* Test the functionality of the given Universal Gates using equivalent 74 series /CD series.	A:14/07/2026 B:08/07/2026 C:13/07/2026	A:21/07/2026 B:15/07/2026 C:20/07/2026		
3	CO2	LLO 3.1	* Construct Basic Gates using Universal Gates.	A:21/07/2026 B:15/07/2026 C:20/07/2026	A:28/07/2026 B:22/07/2026 C:27/07/2026		
4	CO2	LLO 4.1	Construct Exclusive Gates using Universal Gates.	A:28/07/2026 B:22/07/2026 C:27/07/2026	A:04/08/2026 B:29/07/2026 C:03/08/2026		
5	CO2	LLO 5.1	* Verify De-Morgan's Theorem (1 and 2).	A:04/08/2026 B:29/07/2026 C:03/08/2026	A:11/08/2026 B:05/08/2026 C:10/08/2026		
6	CO3	LLO 6.1	* Implement 2 input, 3 input Adder Circuit.	A:11/08/2026 B:05/08/2026 C:10/08/2026	A:18/08/2026 B:12/08/2026 C:17/08/2026		
7	CO3	LLO 7.1	Implement 2 input, 3 input Subtractor Circuit.	A:18/08/2026 B:12/08/2026 C:17/08/2026	A:25/08/2026 B:19/08/2026 C:24/08/2026		
8	CO3	LLO10.1	* Build and test the functionality of 4:1/8:1 Multiplexer. .	A:25/08/2026 B:19/08/2026 C:24/08/2026	A:01/09/2026 B:02/09/2026 C:31/08/2026		
9	CO3	LLO 11.1	Build and test the functionality of 1:4/1:8 De-Multiplexer.	A:01/09/2026 B:02/09/2026 C:31/08/2026	A:08/09/2026 B:09/09/2026 C:07/09/2026		
10	CO3	. LLO 12.1	Implement and verify the truth table of RS Flip flop.	A:08/09/2026	A:15/09/2026		

				B:09/09/2026 C:07/09/2026	B:16/09/2026 C:21/09/2026		
11	CO3	LLO13.1	Implement and test the functionality of master slave- JK Flip Flop using Digital IC.	A:15/09/2026 B:16/09/2026 C:21/09/2026	A:22/09/2026 B:23/09/2026 C:28/09/2026		
12	CO4	LLO 14.1	Use Digital IC to construct and test the functionality of D and T flip flop.	A:22/09/2026 B:23/09/2026 C:28/09/2026	A:29/09/2026 B:30/09/2026 C:05/10/2026		
13	CO4	LLO 16.1	Implement Ripple Counter using Digital IC.	A:29/09/2026 B:30/09/2026 C:05/10/2026	A:06/10/2026 B:07/10/2026 C:12/10/2026		
14	CO4	LLO 17.1	* Implement Decade Counter Using Digital IC.	A:06/10/2026 B:07/10/2026 C:12/10/2026	A:13/10/2026 B:14/10/2026 C:12/10/2026		
15	CO5	LLO 18.1	* Test the output of given R-2R type Digital to Analog Converter for the given input.	A:13/10/2026 B:14/10/2026 C:12/10/2026	A:13/10/2026 B:14/10/2026 C:12/10/2026		

- **Formative Assessment Criteria:**

Performance Indicators		Weightage
Process Related (15 Marks)		**60%**
1	Handling of the components	10%
2	Identification of components	20%
3	Measuring value using suitable instrument	20%
4	Working in teams	10%
Product Related (10 Marks)		**40%**
1	Calculated theoretical values of given component	10%
2	Interpretation of result	05%
3	Conclusions	05%
4	Practical related questions	15%
5	Submitting the journal in time	05%
	Total (25 Marks)	**100%**

• Formative & Summative Assessment Criteria:

1. Formative Assessment (F.A.) of each experiment will be done out of 25 marks on the basis of Tool Selection Ability, Use of Appropriate tool to perform the Identified tasks, Quality of output achieved, Answer to sample questions and Submit report in time total

2. Final term work(FA-PR) of 25 marks is calculated based on scored in Formative Assessment for each experiment
   Term Work Marks = (25* Total Marks Obtained in P.A.) / (25*Total Number of Experiments)

3. Self-learning Activities (SLA) includes micro project / assignment / other activities related to subject and it will be evaluated out of 25 Marks

4. A comprehensive Final Internal Practical examination (SA-PR) of 25 Marks will be conducted by MSBTE at the end of semester. The schedule of MSBTE Practical Examination will be display on Notice board prior to examination.

• Practical wise CO Mapping:

Practical No.	CO302.1	CO302.2	CO302.3	CO302.4	CO302.5
PR. No. 1	✔	✔			
PR. No. 2		✔			
PR. No. 3		✔			
PR. No. 4		✔			
PR. No. 5		✔			
PR. No. 6			✔		
PR. No. 7			✔		
PR. No. 8			✔		
PR. No. 9			✔		
PR. No. 10			✔		
PR. No.11			✔		
PR. No.12				✔	
PR. No.13				✔	
PR. No.14				✔	
PR. No.15				✔	

- **Unit wise CO-PO Mapping:**

Course Outcomes (COs)	Programme Outcomes (POs)							PSOs	
	PO-1 Basic and Discipline Specific Knowledge	PO-2 Problem Analysis	PO-3 Design/ Development of Solutions	PO-4 Engineering Tools	PO-5 Engineering Practices for Society, Sustainability & Environment	PO-6 Project Management	PO-7 Life Long Learning	PSO-1	PSO-2
CO1	2	-	1	-	-	-	3	1	2
CO2	2	-	2	-	-	-	2	2	2
CO3	3	2	3	2	-	1	2	1	1
CO4	3	2	3	2	-	1	2	1	1
CO5	2	-	2	2	1	1	2	2	1

- **Legends:-** High:03, Medium:02, Low:01, --:No Mapping

PSO1: Apply fundamental concepts of Computer Engineering and Artificial Intelligence and machine learning to solve technical problems.

PSO2: Implement the domain knowledge to achieve successful career as an engineering professional

- **References:**

1. Books:

Sr no	Author	Title	Publisher
1	Jain R.P	Modern Digital Electronics	McGraw-Hill Publishing, New Delhi,2009 ISBN:9780070669116
2	Anand Kumar	Fundamentals of Digital Circuits	PHI learning Private limited, ISBN:978-81-203-5268-1
3	Salivahanan S, Arivazhagan S.	Digital Circuits and Design	Vikas Publishing House, New Delhi,2013 ISBN: 9789325960411
4	Puri.V.K	Digital Electronics	McGraw-Hill Publishing, New Delhi,2016 ISBN:97800746331751
5	Malvino A.P Donald .P. Leach	Digital Principles	McGraw-Hill Education, New Delhi ISBN:9789339203405
6	Anil.K.Maini	Digital Electronics: Principles, Devices and Applications	Wiley India, Delhi, 2007, ISBN:9780470032145

2. Web Sites:

Sr. No	Link /Portal	Description
1	https://studytronics.weebly.com/digital-electronics.html	Basics of Digital Electronics
2	https://www.udemy.com/course/basics-of-digital-techniques/	Introduction To Digital Number System & Logic Gates
3	https://www.geeksforgeeks.org/synchronous-sequential-circuits-in-digital-logic/	Boolean Algebra and Logic Gates, Combinational and Sequential Logic Circuits
4	https://onlinecourses.nptel.ac.in/noc19_ee51/preview	Digital Circuits
5	https://de-iitr.vlabs.ac.in/	Virtual Labs for Digital Systems
6	https://www.tutorialspoint.com/digital_circuits/digital_circuits_sequential_circuits.htm	Sequential Circuits
1	https://studytronics.weebly.com/digital-electronics.html	Basics of Digital Electronics

Ms. K.J. Patil
(Name & signature of staff)

.Mrs. R.Y.Thombare
(Name & signature of HOD)

CC- 1. Lab File 2.Course File-BEE 3. Notice Board-MPRL Lab 4. Progressive Assessment